UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,245	10/22/2001	Peter Korger	01-284 1496.00173	2184

24319 7590 01/25/2005

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
FLANAGAN, KRISTA M	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,245	KORGER ET AL.	
	Examiner	Art Unit	
	Krista M. Flanagan	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "apparatus wherein said apparatus is implemented integral to a member selected from a group consisting of an application specific integrated circuit, a CPLD and a FPGA" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

3. The abstract of the disclosure is objected to because the abstract should be a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. This abstract does not. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

5. Claims 1-4, 6, 7, 12-16, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Mackey et al., US Patent Application Publication US 2002/0181631 A1.

6. Regarding claim 1, Mackey discloses an apparatus (See figure 3) comprising: a first circuit (See reference characters 302, 311, 312, 314, 315, 316, 321, 325, 329, and 333) configured to present a first data signal (From reference character 302) and a first indicator signal (enable signal for reference character 304 from reference character 302) in response to a first clock signal (SCLK) and an enable signal (See source event, reference character 333 and page 3, ¶ 0041, lines 6-9, where the even signal is used to indicate when data is available or "valid"); and a second circuit (See reference characters 304, 312, 313, 317, 318, 323, 327, 331, and 335) configured to present a second data signal (From reference character 304) and a second indicator signal (From reference character 304, enable, and page 3, ¶ 0041, lines 6-9) in response to said first data signal, said first indicator signal and a second clock signal (DCLK).

7. Regarding claim 2, which inherits all of the limitations of claim 1, Mackey discloses an apparatus, where the first indicator signal indicates when said first data signal is available for transmission (or valid) and said second indicator signal indicates when said second data signal is valid (See page 3, ¶ 0041, lines 6-13).

8. Regarding claim 3, which inherits all of the limitations of claim 1, Mackey discloses an apparatus where the first clock signal comprises a first logic domain clock signal and said second clock signal comprises a second logic domain clock signal (See figure 3, SCLK, DCLK, and enable signals).

9. Regarding claim 4, which inherits all of the limitations of claim 3, Mackey discloses an apparatus, which is configured to synchronize said second data signal to said second logic domain and where said second data signal comprises said first data signal synchronized to said second domain (See page 1, ¶ 0005).

10. Regarding claim 6, which inherits all of the limitations of claim 1, Mackey discloses an apparatus where the first and second clock signals operate out of phase with each other (See page1, ¶ 0022).

11. Regarding claim 7, which inherits all of the limitations of claim 1, Mackey discloses an apparatus where the first circuit is configured to store said first data signal until a new data signal is received and the second circuit is configured to store said second data signal until said second circuit receives said first data signal (See page 3, ¶ 0041, lines 13-19).

12. Regarding claim 12, which inherits all of the limitations of claim 1, Mackey discloses an apparatus, which is implemented integral to a member selected from a group consisting of an application specific integrated circuit, a CPLD and a FPGA (See page 1, ¶ 0005, lines 1-5).

13. Regarding claim 13, which inherits all of the limitations of claim 1, Mackey discloses an apparatus in which the first and second data signals comprise n-bit wide digital signals, where n is an integer (See page 1, ¶ 0023).

14. Regarding claim 14, Mackey discloses an apparatus comprising: means for presenting a first data signal and a first indicator signal in response to a first clock signal and an enable signal; and means for presenting a second data signal and a second indicator signal in response to said first data signal, said first indicator signal and a second clock signal, wherein said second indicator signal is configured to indicate when said second data signal is synchronized from a first logic domain to a second logic domain (See figure 3 and above rejections to claims 1-3).

15. Regarding claim 15, Mackey discloses a method of indicating data is synchronized from a first logic domain to a second logic domain comprising the steps of presenting a first data

signal and a first indicator signal in response to a first clock signal and an enable signal; and presenting second data signal and to said first data signal, said first second indicator signal in response indicator signal and a second clock signal (See figure 3, and above rejection to claim 1).

16. Regarding claim 16, which inherits all of the limitations of claim 15, Mackey discloses a method wherein the first clock signal comprises a clock signal of a first logic domain and a second clock signal comprises a clock signal of a second logic domain (See page 1, ¶ 0005).

17. Regarding claim 18, which inherits all of the limitations of claim 15, Mackey discloses a method, which further comprises the step of operating said first and second clock signals out of phase with each other (See page 3, ¶ 0022).

18. Regarding claim 19, which inherits all of the limitations of claim 15, Mackey discloses a method, which comprises the step of implementing said method in a member group consisting of an application specific integrated circuit, a CPLD and a FPGA (See page 1, ¶ 0005, lines 1-5).

19. Regarding claim 20, which inherits all of the limitations of claim 15, Mackey discloses a method in which the first and second data signals comprise n-bit wide digital data signals, where n is an integer (See page 1, ¶ 0023).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 5 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mackey in view of Lo et al., US Patent No. 6,247,082. Regarding both claims 5 and 17, Mackey

discloses an apparatus according to claim 1 and a method according to claim 15. Mackey does not disclose an apparatus or method wherein the first and second clock signals operate at the same frequency. Lo discloses a circuit to transact information across multiple clock domains where the clock frequencies could be equal (See column 4, lines 59-64). At the time the invention was made it would have been obvious to one of ordinary skill in the art to use Mackey's apparatus and method for transacting information across multiple clock domains with Lo's specifications where the frequency of the clock signals are the same. One of ordinary skill in the art would have been motivated to do this because it would be advantageous to support all clock frequency configurations.

Allowable Subject Matter

22. Claims 8-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Krista M. Flanagan whose telephone number is (571) 272-2203. The examiner can normally be reached on Monday - Friday, 7 - 3:00.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

kmf
20050118